ABSTRACT OF THE DISCLOSURE

There is disclosed an image read apparatus including an image sensor including: first and second sensors including light receiving devices arranged in one row; a first shift register for outputting the pixel signals of all the light receiving devices of the first sensor; and second and third shift registers for outputting the even numbered and odd numbered pixel signals of the light receiving devices of the second sensor, in which invalid data is prevented from being written in a memory. The pixel signals outputted from the first to third shift registers constituting a CCD image sensor with the same transfer clock are selected and taken in via an AFE in a time division. The taken pixel data is successively sampled in a data sampling block and stored in a memory. Moreover, when the sampling timing is controlled in a take in signal generation circuit, the pixel data stored in the memory is limited to indicate the pixel number of each shift register.